IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-10 (Canceled):

Claim 11 (Original): A semiconductor integrated circuit device, comprising:

a semiconductor substrate with an active region defined by an element isolation region, word lines extending in a first direction over said active region such that gate electrodes of metal insulator semiconductor field effect transistors (MISFETs) are electrically coupled to said word lines, semiconductor regions formed in said active region such that said semiconductor regions serve as a source region or a drain region of each MISFET;

a first insulating film covering said active region, said word lines and said semiconductor regions;

a first opening formed in said first insulating film such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region;

a second opening formed in said first insulating film under said first opening such that, in said first direction, a diameter of said first opening is less than that of said second opening and such that said second opening reaches said semiconductor regions;

a conductive material buried in said first opening and in said second opening; and

a bit line formed over said first insulating film such that said bit line is electrically coupled to said conductive material and extends to cross said word lines.

Claim 12 (Original): A semiconductor integrated circuit device according to claim 11, further comprising:

a capacitor element formed over said first insulating film;

a third opening formed in said first insulating film to reach other semiconductor region; and

a conductive material buried in said third opening,

wherein said capacitor element is electrically coupled to the other semiconductor region through said conductive material buried in said third opening.

Claim 13 (Original): A semiconductor integrated circuit device according to claim 12, wherein a memory cell of a dynamic random access memory is comprised of said MISFET and said capacitor element.

Claim 14 (New): A semiconductor integrated circuit device, comprising:

a semiconductor substrate provided with an active region defined by an element isolation region, word lines extending in a first direction over said active region such that gate electrodes of metal insulator semiconductor field effect transistors (MISFETs) are electrically coupled to said word lines, semiconductor

regions formed in said active region such that said semiconductor regions serve as a source region or a drain region of each MISFET;

a first insulating film deposited over said active region, said word lines and said semiconductor regions;

a first opening formed in said first insulating film such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region;

a second opening formed in said first insulating film under said first opening such that, in said first direction, a diameter of said first opening is less than that of said second opening and such that said second opening reaches said semiconductor region;

a third opening formed in said first insulating film to reach other semiconductor region;

a conductive material buried in said first opening, said second opening, and said third opening; and

a bit line formed over said first insulating film such that said bit line is electrically coupled to said conductive material and extends to cross said word lines.

Claim 15 (New): A semiconductor integrated circuit device according to claim 14, further comprising:

a capacitor element formed over said first insulating film,

wherein said capacitor element is electrically coupled to said other semiconductor region through said conductive material buried in said third opening.

Claim 16 (New): A semiconductor integrated circuit according to claim 14, wherein a memory cell of a dynamic random access memory is comprised of said MISFET and said capacitor element.